SEOKHYEONG KANG

Contact Information

Pohang University of Science and Technology (POSTECH)
Department of Electrical Engineering, 77 Chungam-Ro, Nam-Gu, Pohang
37673, Republic of Korea

Phone: +82-10-4225-7480
E-mail: shkang@postech.ac.kr
http://soc.postech.ac.kr

Education

- Ph.D. in Electrical and Computer Engineering
  University of California, San Diego (Sep. 2008 - Aug. 2013)
  Advisor: Prof. Andrew B. Kahng
- M.Sc. in Electrical Engineering
  Pohang University of Science and Technology, Pohang, South Korea (Mar. 1999 - Feb. 2001)
- B.Sc. in Electrical Engineering
  Pohang University of Science and Technology, Pohang, South Korea (Mar. 1995 - Feb. 1999)

Professional Experience

- **Pohang University of Science and Technology (POSTECH) (Mar. 2018 – present)**
  Associate Professor
  - VLSI CAD (physical design optimization), System-on-Chip Design
- **Ulsan National Institute of Science and Technology (UNIST) (Aug. 2014 – Mar. 2018)**
  Assistant Professor
  - Low-power System-on-Chip Design:
- **ASIC Design Automation, Qualcomm Technologies, Inc. (Aug. 2013 – Aug. 2014)**
  Staff Engineer
  - Low-power design methodology development
- **VLSI CAD Laboratory, University of California, San Diego (Sep. 2008 - Aug. 2013)**
  - System-aware low-power design methodology / Low-Power design implementation and optimization
  - Thesis: Low-Power Integrated-Circuit Implementation Exploiting System and Application Information
- **SoC Development Team, Samsung Co., LTD., South Korea (Feb. 2001 - July 2008)**
  Senior Engineer
  - Development of Blu-ray/HD-DVD recorder SoC (system architecture, SATA IF, ECC)
- **CAD & SoC Design Lab., POSTECH, Pohang, South Korea (Mar. 1999 - Feb. 2001)**
  Thesis: Area Optimization of the Cell-based Design

Publications

- All papers with Prof. Andrew B. Kahng, have authors listed in alphabetical order.

Journal

[1] Andrew B. Kahng, **Seokhyeong Kang**, Seungwon Kim, and Bangqi Xu, "Enhanced Power Delivery Pathfinding for Emerging 3D Integration Technology", *IEEE TVLSI* (2020)

[2] Hwa-Pyeong Park, Yesung Kang, **Seokhyeong Kang**, and Jee-Hoon Jung, "FPGA Controller Design for High-Frequency LLC Resonant Converters", *Institute of Electrical Engineers of Japan (IEEJ)* (2020).

[3] Sunmean Kim, Sung-Yun Lee, Sunghye Park, Kyung Rok Kim, and **Seokhyeong Kang**, "A Logic Synthesis Methodology for Low-Power Ternary Logic Circuits", *IEEE TCAS-I* (2020).

[4] Sodam Han, Yonghee Yun, Young Hwan Kim, and **Seokhyeong Kang**, "Proactive Scenario Characteristic-aware Online Power Management on Mobile Systems", *IEEE Access* (2020).

[5] Hyunjeong Kwon, Sung-Yun Lee, Young Hwan Kim, and **Seokhyeong Kang**, "Additive Statistical Leakage Analysis Using Exponential Mixture Model", *IEEE TCAD* (2020).

[6] Ho Sub Lee, Gyujin Bae, Sung In Cho, Young Hwan Kim, and **Seokhyeong Kang**, "SmartGrid: Video Retargeting with Spatiotemporal Grid Optimization", *IEEE Access* 7 (2019), pp. 127564-127579.

[7] Seungwon Kim, Ki Jin Han, Youngmin Kim and **Seokhyeong Kang**, "Power Integrity Coanalysis Methodology for Multi-Domain High-Speed Memory Systems", *IEEE Access* 7 (2019), pp. 95305-95313.

[8] Daeyeon Kim, SangGi Do, Sung-Yun Lee and **Seokhyeong Kang**, "Compact Topology-aware Bus Routing for Design Regularity", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2019)

[9] Hyunjeong Kwon, Jae Hoon Kim, **Seokhyeong Kang** and Young Hwan Kim, "SoftCorner: Relaxation of Corner Values for Deterministic Static Timing Analysis of VLSI Systems", *IEEE Access* 6 (2018), pp. 60115-60127.

[10] Sunwoo Heo, Sunmean Kim, Kiyung Kim, Hyeji Lee, So-Young Kim, Yun Ji Kim, Seung Mo Kim, Ho-In Lee, Kyung Rok Kim, **Seokhyeong Kang** and Byoung Hun Lee, "Ternary full adder using multi-threshold voltage graphene barristors", *IEEE Electron Device Letters* 39 (2018), pp. 1948-1951.

[11] Hyunjeong Kwon, Mingyu Woo, Young Hwan Kim and **Seokhyeong Kang**, "Statistical Leakage Analysis Using Gaussian Mixture Model", *IEEE Access* 6 (2018), pp. 51939-51950.

[12] Seungwon Kim, **Seokhyeong Kang**, Ki Jin Han and Youngmin Kim, "Novel Adaptive Power Gating Strategy and Tapered TSV Structure in Multi-layer 3D IC", *ACM Transactions on Design Automation of Electronic Systems* 21(3) (2016), pp. 44:1-44:19.

[13] Sangmin Kim, Seungwhun Paik, **Seokhyeong Kang** and Youngsoo Shin, "Wakeup Scheduling and Its Buffered Tree Synthesis for Power Gating Circuits", *Integration, the VLSI journal* 53(C) (2016), pp. 157-170.

[14] Sangmin Kim, **Seokhyeong Kang** and Youngsoo Shin, "Synthesis of Dual-Mode Circuits through Library Design, Gate Sizing, and Clock Tree Optimization", *ACM Transactions on Design Automation of Electronic Systems* 21(3) (2016), pp. 51:1- 51:23.

[15] Andrew B. Kahng, **Seokhyeong Kang**, Jiajia Li and Jose Pineda De Gyvez, "An Improved Methodology for Resilient Design Implementation", *ACM Transactions on Design Automation of Electronic Systems* 20(4) (2015), pp. 1-26.

[16] Andrew B. Kahng, **Seokhyeong Kang**, Tajana S. Rosing and Richard Strong, "Many-Core Token-Based Adaptive Power Gating", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 32(8) (2013), pp. 1288–1292.

[17] Andrew B. Kahng, **Seokhyeong Kang**, Rakesh Kumar and John Sartori, "Enhancing the Efficiency of Energy-Constrained DVFS Designs", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 21(10) (2013), pp. 1769–1782.

[18] Andrew B. Kahng, **Seokhyeong Kang**, Rakesh Kumar and John Sartori, "Recovery-Driven Design: Exploiting Error Resilience in Design of Energy-Efficient Processors", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 31(3) (2012), pp. 404–417.

Conference

[1] Yesung Kang, Eunji Kwon, Seunggyu Lee, Younghoon Byun, Youngjoo Lee and **Seokhyeong Kang**, "Approach to Improve the Performance Using Bit-level Sparsity in Neural Networks", Proc. Design, Automation and Test in Europe, 2021, to appear.

[2] Daeyeon Kim, Hyunjeong Kwon, Sung-Yun Lee, Seungwon Kim, Mingyu Woo and **Seokhyeong Kang**, "Machine Learning Framework for Early Routability Prediction with Artificial Netlist Generator", *Proc. Design, Automation and Test in Europe*, 2021, to appear.

[3] Sunghoon Kim, Hyunjeong Kwon, Eunji Kwon, Youngchang Choi, Taehyun Oh and Seokhyeong Kang, "MDARTS: Multi-objective Differentiable Neural Architecture Search", *Proc. Design, Automation and Test in Europe*, 2021, to appear.

[4] Yoonho Park, Yesung Kang, Sunghoon Kim, Eunji Kwon, and **Seokhyeong Kang**, "GRLC: Grid-based Run-length Compression for Energy-efficient CNN Accelerator", *Proc. IEEE International Symposium on Low Power Electronics and Design*, 2020 (Best Paper Award)

[5] Eunji Kwon, Sodam Han, Yoonho Park, Young Hwan Kim, and **Seokhyeong Kang**, "Late Breaking Results: Reinforcement Learning-based Power Management Policy for Mobile Device Systems", *Proc. ACM/IEEE Design Automation Conference*, 2020.

[6] Kiyung Kim, Sunmean Kim, Yongsu Lee, Daeyeon Kim, So-Young Kim, **Seokhyeong Kang**, and Byoung Hun Lee, "Extreme Low Power Technology using Ternary Arithmetic Logic Circuits via Drastic Interconnect Length Reduction", *Proc. IEEE International Symposium on Multiple-Valued Logic*, 2020.

[7] Yesung Kang, Yoonho Park, Sunghoon Kim, Eunji Kwon, Taeho Lim, Sangyun Oh, Mingyu Woo, and **Seokhyeong Kang,** "Analysis and Solution of CNN Accuracy Reduction over Channel Loop Tiling", *Proc. Design Automation and Test in Europe*, 2020.

[8] SangGi Do, Mingyu Woo, **Seokhyeong Kang**, "Fence-Region-Aware Mixed-Height Standard Cell Legalization", Proc. Great Lakes Symposium on VLSI, 2019, pp. 259-262.

[9] Sunmean Kim, Sung-Yun Lee, Sunghye Park and **Seokhyeong Kang**, "Design of Quad-Edge-Triggered Sequential Logic Circuits for Ternary Logic", *Proc. IEEE International Symposium on Multiple-Valued Logic*, 2019, pp. 37-42.

[10] Sung-Yun Lee, Sunmean Kim and **Seokhyeong Kang**, "Ternary Logic Synthesis with Modified Quine-McCluskey Algorithm", *Proc. IEEE International Symposium on Multiple-Valued Logic*, 2019, pp. 158-163.

[11] Andrew B. Kahng, **Seokhyeong Kang**, Seungwon Kim, Kambiz Samadi and Bangqi Xu, "Power Delivery Pathfinding for Emerging Die-to-Wafer Integration Technology", *Proc. Design, Automation and Test in Europe*, 2019, pp. 842–847.

[12] Seungwon Kim and **Seokhyeong Kang**, "Fast Chip-Package-PCB Coanalysis Methodology for Power Integrity of Multi-domain High-Speed Memory: A Case Study", Proc. IEEE/ACM Design, Automation and Test, in Europe, 2018, pp. 885–888.

[13] Sunmean Kim, Taeho Lim and **Seokhyeong Kang**, "An Optimal Gate Design for the Synthesis of Ternary Logic Circuits", *Proc. Asia and South Pacific Design Automation Conference*, 2018, pp. 476 – 481.

[14] Mingyu Woo, Seungwon Kim and **Seokhyeong Kang**, "GRASP based Metaheuristics for Layout Pattern Classification", *Proc. IEEE/ACM International Conference on Computer-Aided Design*, 2017, pp. 512-518.

[15] Seungwon Kim, SangGi Do and **Seokhyeong Kang**, "Fast Predictive Useful Skew Methodology for Timing-Driven Placement Optimization", *Proc. ACM/IEEE Design Automation Conference*, 2017, pp. 18-23.

[16] Yesung Kang, Jaewoo Kim, Sunmean Kim, Sunhae Shin, E-San Jang, Jae Won Jeong, Kyung Rok Kim and **Seokhyeong Kang**, "A Novel Ternary Multiplier based on Ternary CMOS Compact Model", *Proc. IEEE International Symposium on Multiple-Valued Logic*, 2017, pp 25-30.

[17] Yesung Kang, Jaewoo Kim and **Seokhyeong Kang**, "A Novel Approximate Synthesis Flow for the Energy-Efficient FIR filter", Proc. IEEE International Conference on Computer Design, 2016, pp. 96-102.

[18] Jaemin Lee, Sunmean Kim, Youngmin Kim and **Seokhyeong Kang**, "A Novel Design Methodology for Error-resilient Circuits in Near-threshold Computing", *Proc. IEEE International Conference on Consumer Electronics-Asia*, 2016, pp. 1-4.

[19] SangGi Do, Seungwon Kim, and **Seokhyeong Kang**, "Skew control methodology for useful-skew implementation", *Proc. International SoC Design Conference*, 2016, pp. 221-222.

[20] Jaemin Lee, Seungwon Kim, Youngmin Kim and **Seokhyeong Kang**, "An Optimal Operating Point by Using Error Monitoring Circuits with An Error-Resilient Technique", *Proc. IFIP/IEEE International Conference on Very Large Scale Integration*, 2015, pp.69-73.

[21] Seungwon Kim, Ki Jin Han, **Seokhyeong Kang** and Yougming Kim, "Novel Adaptive Power Gating Strategy of TSV-based Multi-layer 3D IC", *Proc. IEEE International Symposium on Quality Electronic Design*, 2015, pp. 537-541.

[22] Seungwon Kim, Ki Jin Han, **Seokhyeong Kang** and Youngmin Kim, "Analysis and Reduction of Voltage Noise of Multi-layer 3D IC with PEEC-based PDN and Frequency-dependent TSV models", *Proc. IEEE International SoC Design Conference*, 2014, pp. 124-125.

[23] Andrew B. Kahng, **Seokhyeong Kang** and Jiajia Li, "A New Methodology for Reduced Cost of Resilience", *Proc. Great Lakes Symposium on VLSI*, 2014, pp. 157-162.

[24] Andrew B. Kahng, **Seokhyeong Kang**, Hyein Lee, Igor L. Markov and Pankit Thapar, "High-Performance Gate Sizing with a Signoff Timer", *Proc. IEEE/ACM International Conference on Computer-Aided Design*, 2013, pp. 450–457.

[25] Wei-Ting Chan, Andrew B. Kahng, **Seokhyeong Kang**, Rakesh Kumar and John Sartori, "Statistical Analysis and Modeling for Error Composition in Approximate Computation Circuits", *Proc. IEEE International Conference on Computer Design*, 2013, pp. 47–53.

[26] Andrew B. Kahng, **Seokhyeong Kang** and Hyein Lee, "Smart Non-Default Routing for Clock Power Reduction", *Proc. ACM/IEEE Design Automation Conference*, 2013, pp. 91.1–91.7.

[27] Andrew B. Kahng, **Seokhyeong Kang**, Hyein Lee, Siddhartha Nath and Jyoti Wadhwani, "Learning-Based Approximation of Interconnect Delay and Slew in Signoff Timing Tools", *Proc. IEEE System-Level Interconnect Prediction*, 2013.

[28] Andrew B. Kahng, **Seokhyeong Kang** and Bongil Park, "Active-Mode Leakage Reduction with Data-Retained Power Gating", *Proc. IEEE/ACM Design, Automation and Test in Europe*, 2013, pp. 1209–1214.

[29] Jin Hu, Andrew B. Kahng, **Seokhyeong Kang**, Myung-Chul Kim and Igor L. Markov "Sensitivity-Guided Metaheuristics for Accurate Discrete Gate Sizing", *Proc. IEEE/ACM International Conference on Computer-Aided Design,* 2012, pp. 233–239.

[30] Andrew B. Kahng, **Seokhyeong Kang**, Tajana S. Rosing and Richard Strong, "TAP - Token-Based Adaptive Power Gating", *Proc. International Symposium on Low Power Electronics and Design*, 2012, pp. 203–208.

[31] Andrew B. Kahng and **Seokhyeong Kang**, "Accuracy-Configurable Adder for Approximate Arithmetic Designs", *Proc. ACM/IEEE Design Automation Conference*, 2012, pp. 820–825.

[32] Andrew B. Kahng and **Seokhyeong Kang**, "Construction of Realistic Gate Sizing Benchmarks With Known Optimal Solutions", *Proc. ACM International Symposium on Physical Design*, 2012, pp. 153–160.

[33] Kwangok Jeong, Andrew B. Kahng, **Seokhyeong Kang**, Tajana S. Rosing and Richard Strong, "MAPG: Memory Access Power Gating", *Proc. IEEE/ACM Design, Automation and Test in Europe*, 2012, pp. 1054–1059.

[34] Andrew B. Kahng, **Seokhyeong Kang**, Rakesh Kumar and John Sartori, "Recovery-Driven Design: A Power Minimization Methodology for Error-Tolerant Processor Modules", *Proc. ACM/IEEE Design Automation Conference*, 2010, pp. 825–830.

[35] Kwangok Jeong, Andrew B. Kahng and **Seokhyeong Kang**, "Toward Effective Utilization of Timing Exceptions in Design Optimization", *Proc. International Symposium on Quality Electronic Design*, 2010, pp. 54–61.

[36] Andrew B. Kahng, **Seokhyeong Kang**, Rakesh Kumar and John Sartori, "Designing a Processor From the Ground Up to Allow Voltage/Reliability Tradeoffs", *Proc. International Symposium on High-Performance Computer Architecture*, 2010, pp. 119–129.

[37] Andrew B. Kahng, **Seokhyeong Kang**, Rakesh Kumar and John Sartori, "Slack Redistribution for Graceful Degradation Under Voltage Overscaling", *Proc. IEEE Asia and South Pacific Design Automation Conference*, 2010, pp. 825–831.

Patent

[1] **Seokhyeong Kang**, "Device and Method for Determining a Defective Area on an Optical Media" U.S. 7849379, Taiwan 2006-38413, Japan 2006-164503, France 2879011-A1.

[2] **Seokhyeong Kang**, "Defect Judgment Apparatus for the Optimized Defect Process of an Optical Storing Medium", Korea 102004-0102362.

[3] B. I. Park, A. B. Kahng, **S. H. Kang** and J. G. Lee, "Data-Retained Power-Gating Circuit and Devices Including the Same", U.S. Patent No. 9,166,567, October 20, 2015.

[4] Andrew B. Kahng and **Seokhyeong Kang**, "Accuracy Configurable Adders and Methods", U.S. 9229686.

[5] **Seokhyeong Kang**, Sunmean Kim and Taeho Lim, "Apparatus for Ternary Logic Circuit" Korea 10-1928223.

[6] **Seokhyeong Kang** and Yesung Kang, "FIR Filter Calculation Method using Approximate Synthesis" Korea 10-1878400.

[7] **Seokhyeong Kang**, Yesung Kang, Yoonho Park and Seonghoon Kim, "NEURAL NETWORK ACCELERATOR AND OPERATING METHOD THEREOF", U.S. UP-2900650-US

[8] **Seokhyeong Kang,** Sungyun Lee, and Sunmean Kim, "APPARATUS AND METHOD FOR TERNARY LOGIC SYNTHESIS WITH MODIFIED QUINE-MCCLUSKEY ALGORITHM", U.S. 20200210637

Awards and Honors

- 10-Year Retrospective Most Influential Paper Award, ASP-DAC 2020
- Third place at the ICCAD CAD Contest (LED/DEF Based Open-Source Global Router), 2019
- Third place at the ISPD Initial Detailed Routing Contest, 2019
- First place (Metric #2) and second place (Metric #1) at the ISPD Discrete Gate Sizing Contest, 2013

Professional Activities

- ACM SIGDA Korea Chapter: Chair, 2019 – present
- ACM SIGDA Korea Chapter: Secretary/Treasurer, 2014 – 2018
- IEEE International SoC Design Conference: Organizing Committee/ Technical Program Committee, 2015 – 2019
- IEEE Asia and South Pacific Design Automation Conference: General Chair Secretary, 2018
- IEEE Asia Pacific Conference on Circuits and Systems: Local Arrangement Chair, 2016
- IFIP/IEEE International Conference on Very Large Scale Integration: Local Arrangement Chair, 2015