CAD & SoC Design Lab.

Lab. Intro.

Seokhyeong Kang

Associate Professor, Ph.D.

CAD & SoC Design Lab.
Department of Electrical Engineering
Pohang University of Science and Technology (POSTECH)

Prof. Seokhyeong Kang: Research and Industry Experiences

2018 POSTECH
2014 UNIST
2013 QUALCOMM
2008 UC San Diego
2001 SAMSUNG
1999 POSTECH
1995

Seokhyeong Kang

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E-mail : shkang@postech.ac.kr

LinkedIn

Google Scholar

Resume

Professional Experience

- Associate Professor in POSTECH (Mar. 2018 ~ Present)
- Assistant Professor in UNIST (Aug. 2014 ~ Mar. 2018)

Research Experience

- Staff Engineer, ASIC Design Automation, Qualcomm Technologies, Inc. (Aug. 2013 ~ Aug. 2014)
- Senior Engineer, SoC Development Team, Samsung Co., LTD., (Feb. 2001 ~ July 2008)

Education

- Ph.D in Electrical and Computer Engineering, University of California, San Diego (Sep. 2008 ~ Aug. 2013), Advisor: Prof. Andrew B. Kahng
- M.Sc. in EE, POSTECH, Pohang (Mar. 1999 ~ Feb. 2001), Advisor: Prof. Young Hwan Kim
- B.Sc. in EE, POSTECH, Pohang (Mar. 1995 ~ Feb. 1999)

CAD & SoC Design Lab. – Members (25)

권민혁
통합 6년차

최영창
박사 4년차

윤종호
통합 5년차

민경준
통합 5년차

임재경
통합 5년차

이자강
박사 3년차

조진오
박사 2년차

서재민
통합 4년차

박성현
통합 4년차

이재승
통합 4년차

김준석
박사 1년차

조규민
통합 3년차

박현우
석사 2년차

장성규
석사 2년차

서준영
통합 2년차

안진모
석사 2년차

국명준
석사 2년차

남종현
석사 2년차

김세현
통합 1년차

이성열
통합 1년차

정윤석
석사 1년차

이대현
석사 1년차

장호우
석사 1년차

박제영
석사 1년차

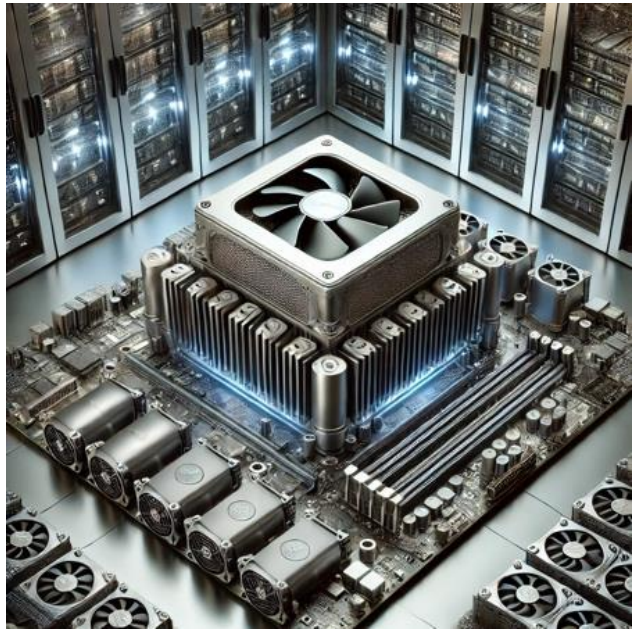
장준환
석사 1년차

CAD & SoC Design Lab. – Research Topics

Electronic Design Automation

휴리스틱 알고리즘과 AI 기술을 활용하여 디자인의 파워, 성능, 면적 (PPA)를 최적화하기 위한 연구 수행

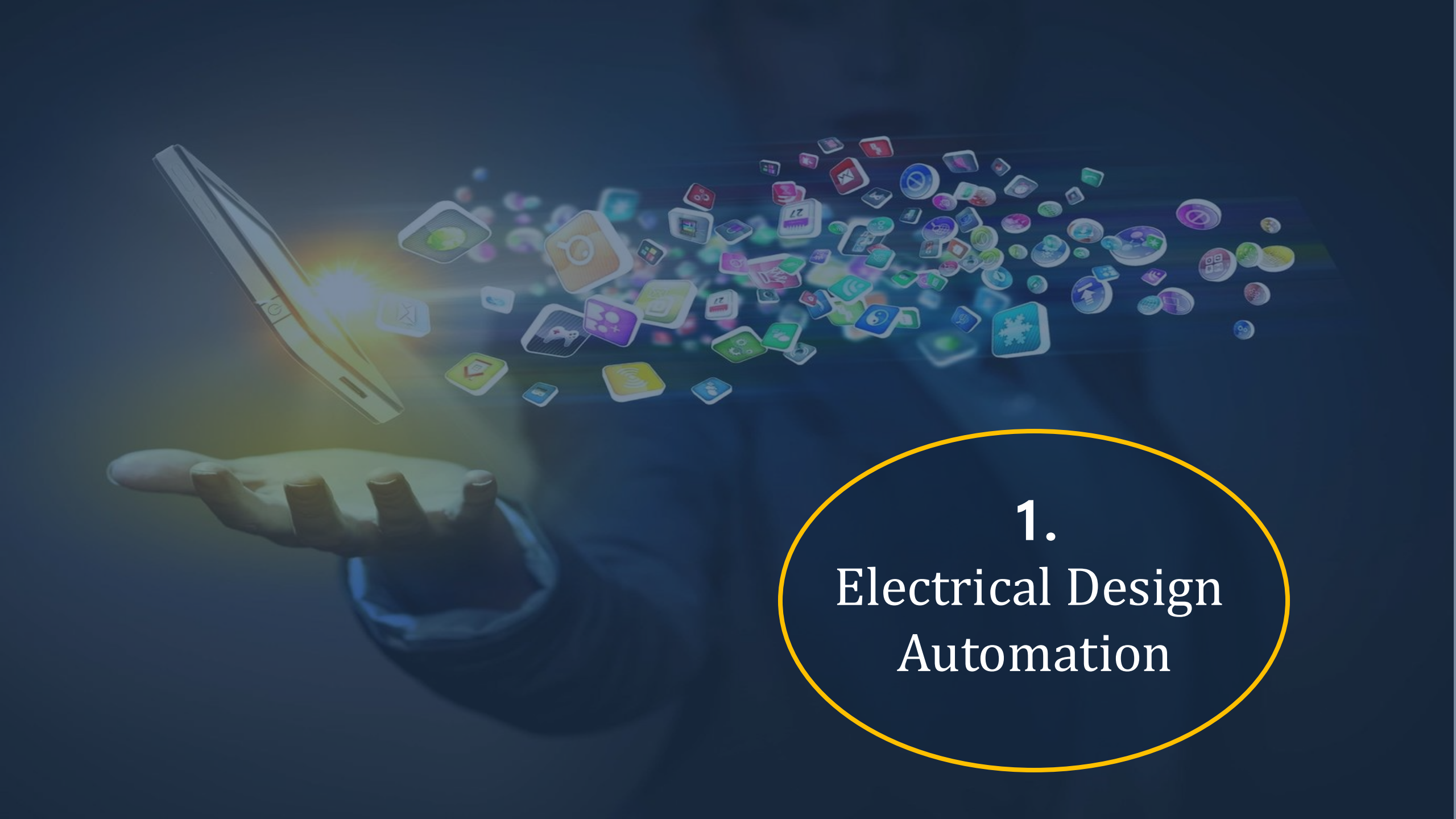
#Physical Design, DTCO, DSO



Deep-learning Hardware

딥러닝 모델 (CNN, Transformer 등)의 연산을 가속하기 위한 하드웨어 및 소프트웨어에 대한 연구 수행

#Parallel Processing, Model Compression, Pruning

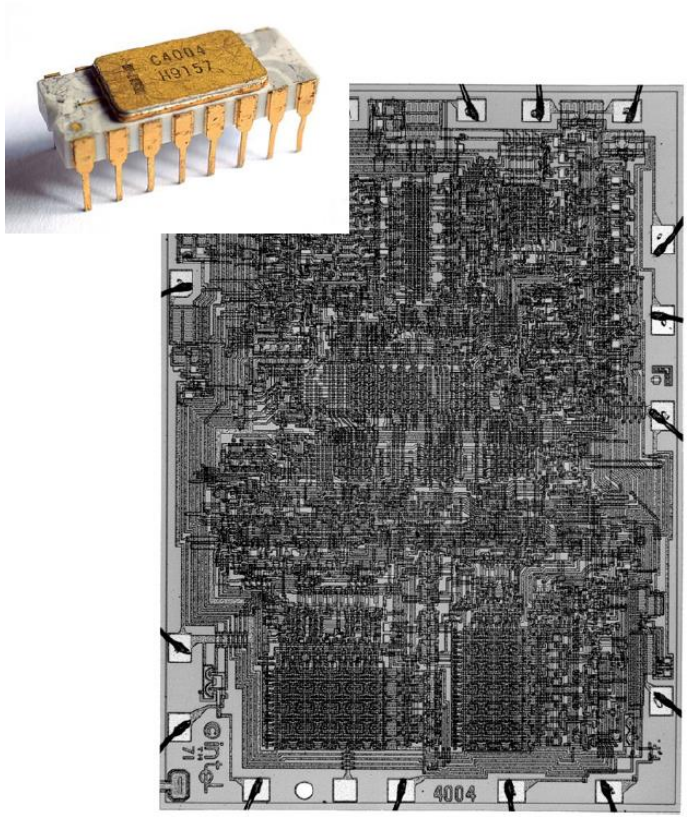


1.
Electrical Design Automation

Development of IC Design

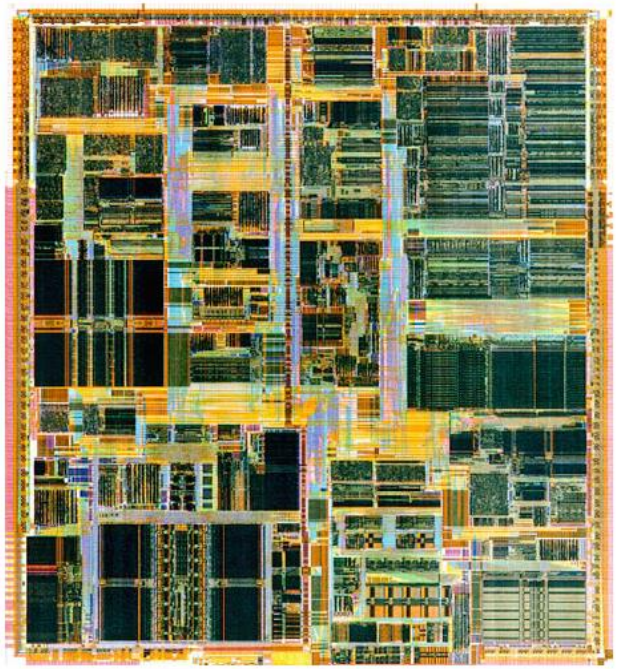
Intel 4004 vs. Intel 14nm CPU

3,500X performance
90,000X energy efficiency
60,000X low cost per Tr.



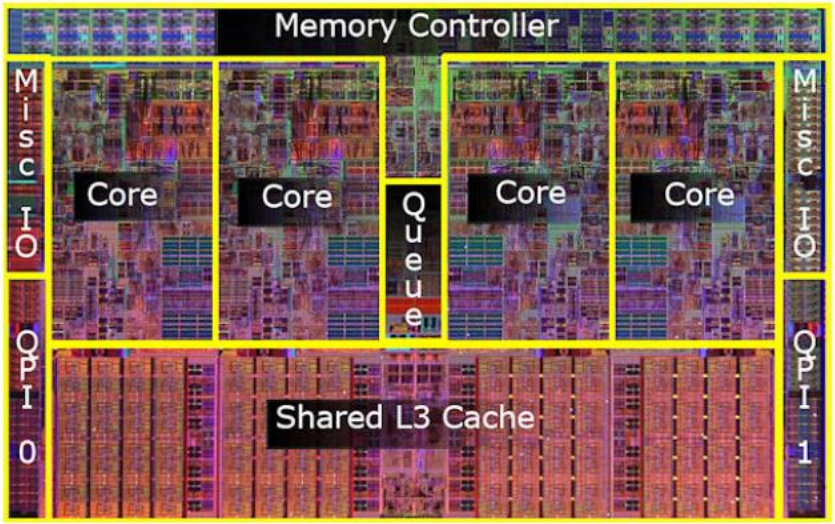
Intel 4004 (1971)

~ 1000 transistors



Pentium 4 (2000)

~ 125M transistors



Core i7 (2010)

~ 731M transistors

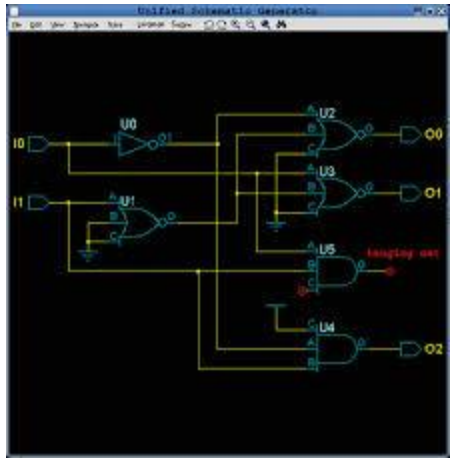
Electronic Design Automation (EDA)

- Electronic design automation (EDA) is a category of SW tools for designing electronic systems such as integrated circuits.
- Billions of components in modern semiconductor chip → **EDA tools** are essential.

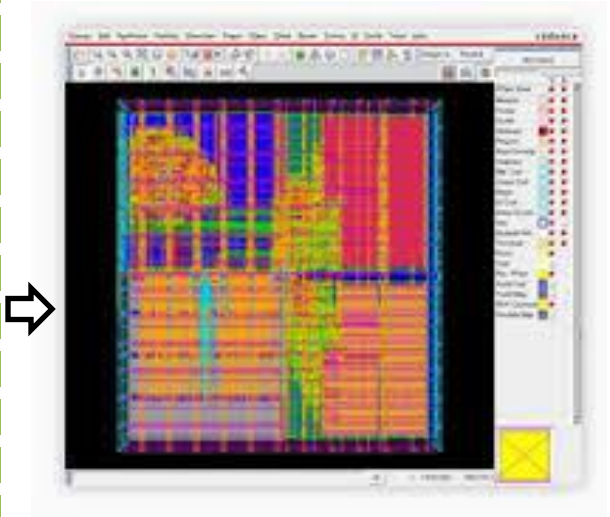
EDA Workflow

```
module TwoDepthDelay(
           input dataIn,
           input clk,
           input reset,
           output reg dataOut);

reg intermediate;

always @(posedge clk or posedge reset)
begin
   if(reset)
   begin
      dataOut      <= 1'b0;
      intermediate <= 1'b0;
   end
   else
   begin
      intermediate <= dataIn;
      dataOut      <= intermediate;
   end
end

endmodule
```

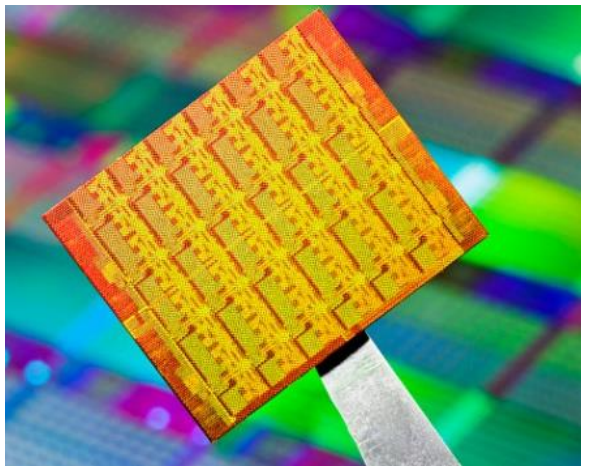
HDL code



Gate-level netlist



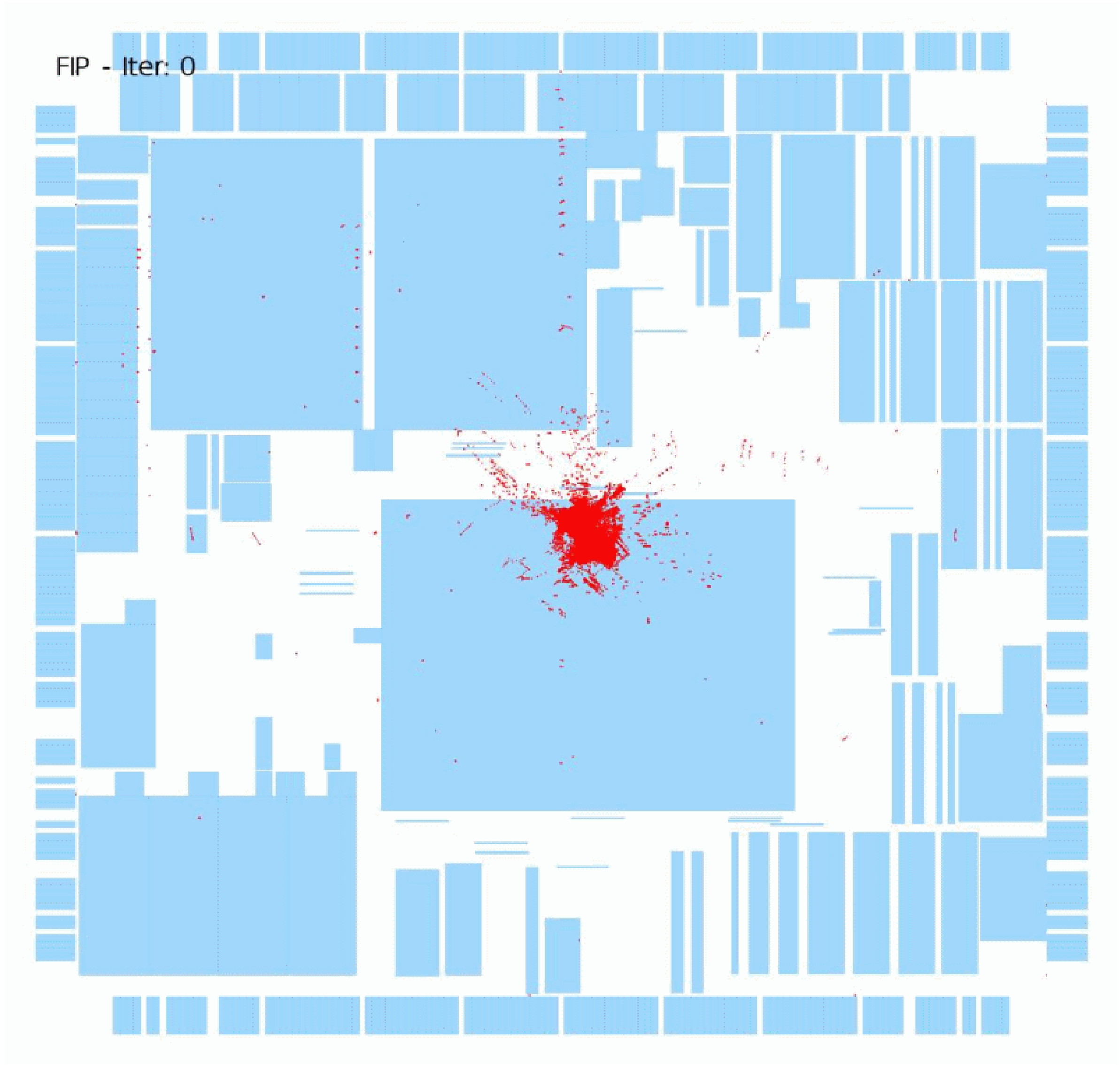
Physical layout

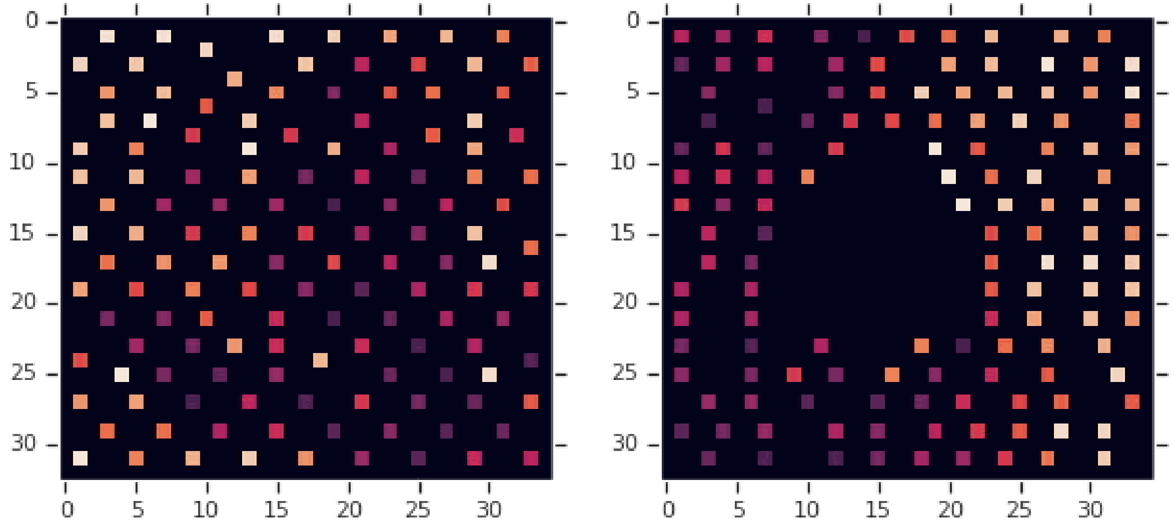


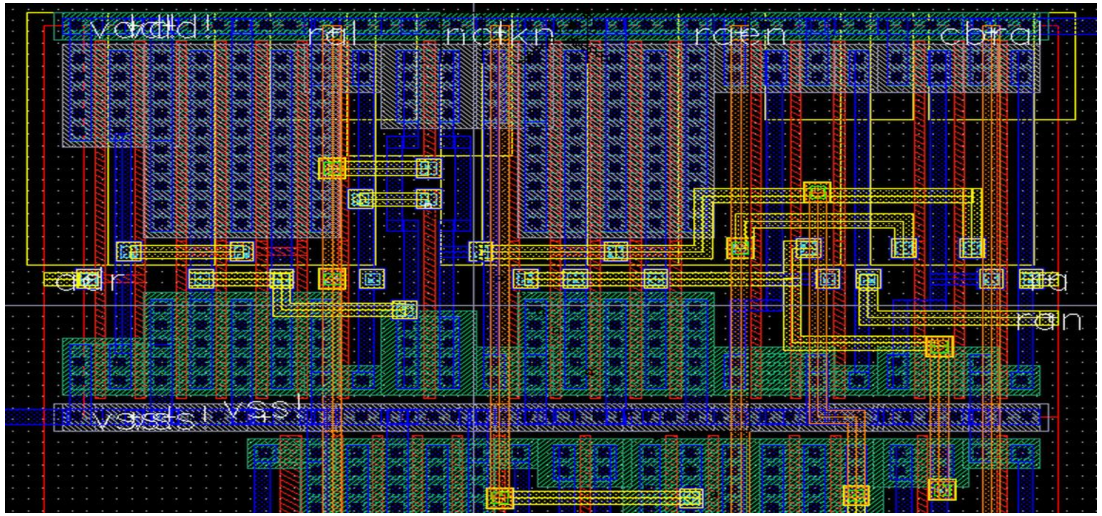
Integrated circuit

Logic Synthesis **Physical Design** **Verification/Test**

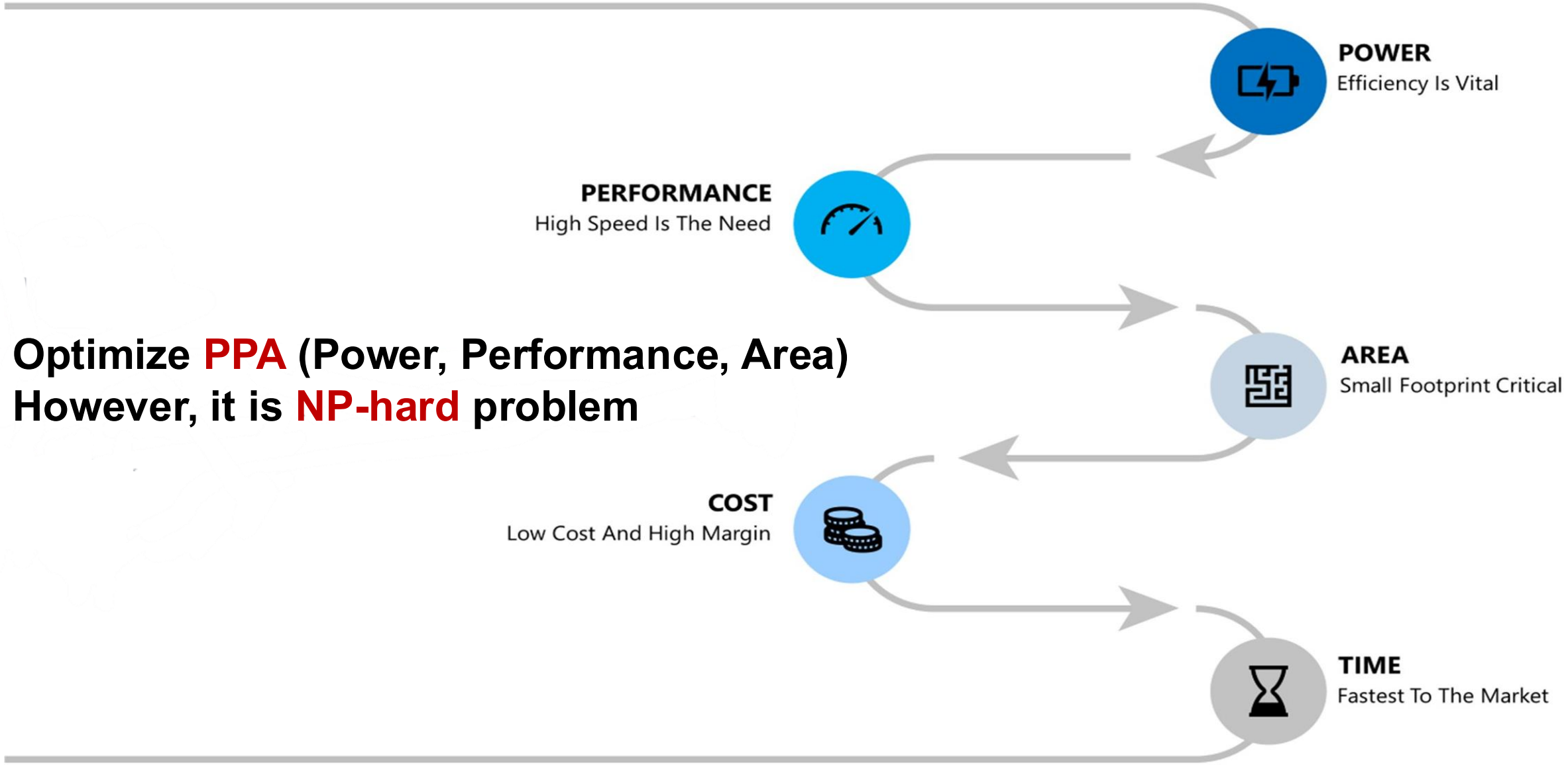
EDA Tools







Goal of EDA



Optimize PPA (Power, Performance, Area)
However, it is NP-hard problem

https://mobile.twitter.com/iChetanPatil/status/1342563617305026560/photo/1

Machine Learning in EDA

Limit of Existing EDA tool

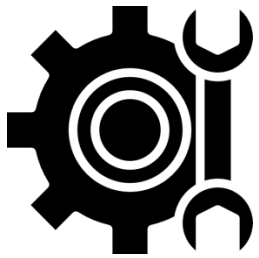
- **Heuristic**: Uses experience or intuition to infer sufficiently efficient answers
- **Deterministic**: All decisions are repeatable (Not random)

→ **High possibility of falling into a local minimum, not global minimum**

Why Machine Learning?

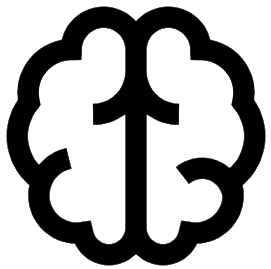
- **Search Space** ⇈ → Possibility of finding Global minimum ⇈
- **Turn-around Time** ⇊ → Time and cost of designing a chip ⇊

ML EDA Framework



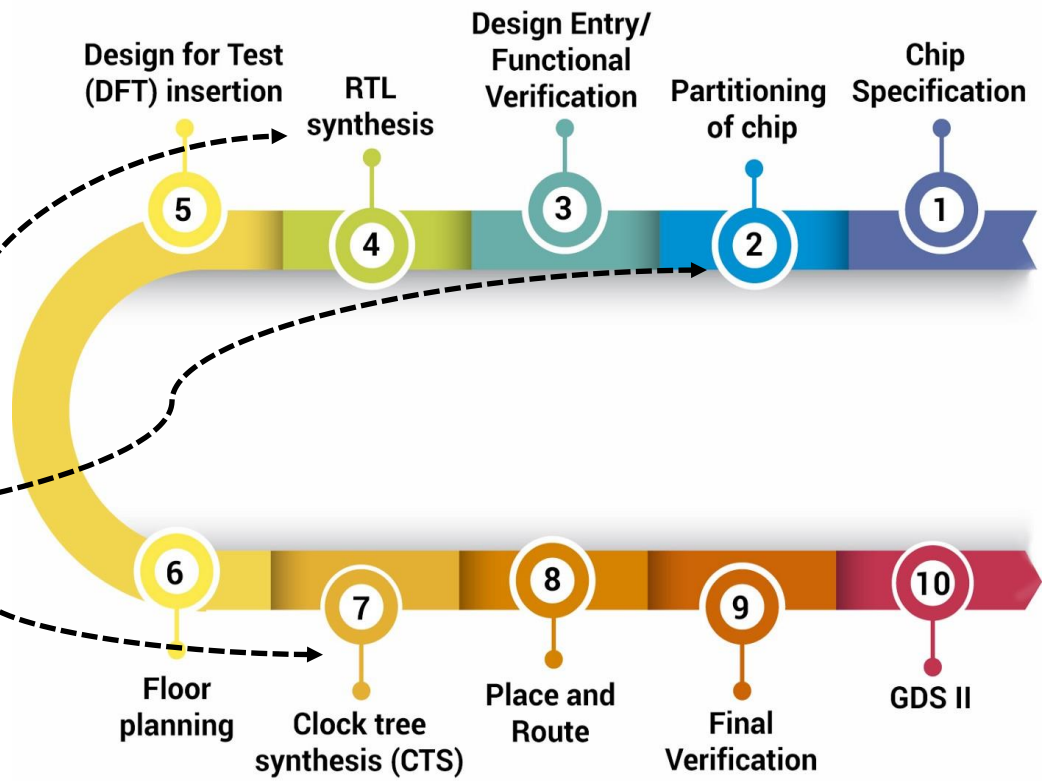
EDA Tools

Feature Data



Machine Learning Model

Application

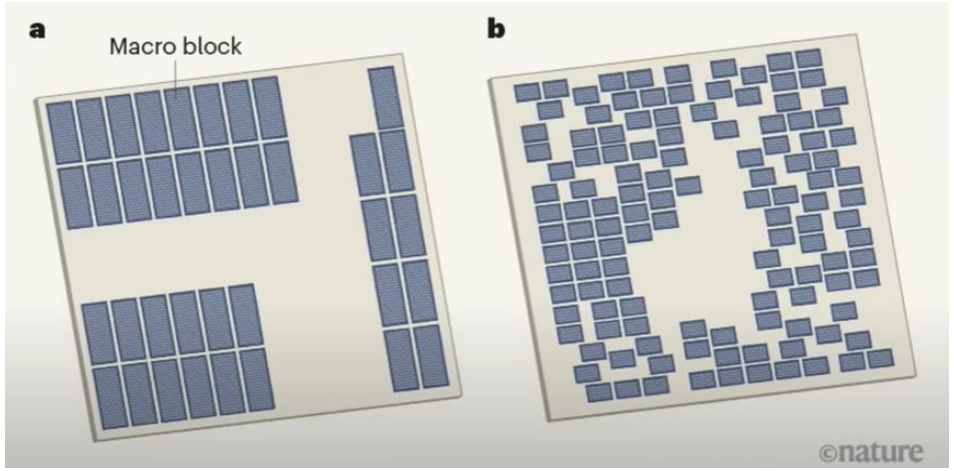


Machine Learning in EDA

구글, 반도체 설계에 AI 적용..."수개월 걸리던 작업을 6시간 만에"

김동원 기자 입력 2021.06.10 14:26 수정 2021.06.30 12:01 댓글 0 좋아요 0

구글, 국제 학술지 네이처에 AI로 TPU V4 설계했다고 밝혀
사람이 수개월 걸려 하던 '평면 배치'에 AI 적용...작업 6시간 만에 끝내
자율주행차·5G·AI 개발 속도 높아질 것으로 기대
"설계 빨라진 만큼, 생산시설 확보도 중요"



Recently-Published AI-EDA Works from POSTECH CSDL (2023)

Custom Design → **DTCO/DSO** → **Placement** → **Routing** → **Sign-off**

RL-based Analog Circuit Optimization

(DATE 2023, DAC 2023)

- Reduce the number of simulations and improve FoM with multi-actors and gm/ID sizing

ML-based SPICE Simulation

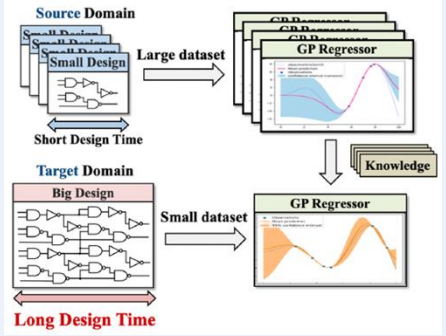
(MLCAD 2023)

- Predict SPICE simulation of analog circuit array using Conv-LSTM

Cell auto-tuning

(ISLPED 2023)

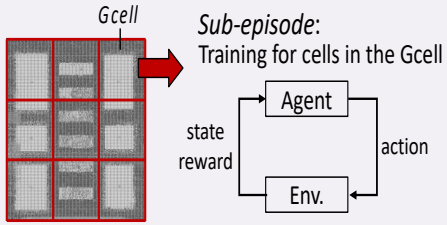
- Find the optimal design & technology parameters (VDD, Vth, Cell height)
- Gaussian process & Transfer learning from small source design to large target design



RL-Legalizer

(DATE 2023)

- Improve sequential std. cell placement with RL
- Grid-based cell feature extraction



Netlist Clustering

(ICCAD 2023)

- Netlist clustering and prediction for each cluster

NetGen

(TCAD 2023)

- Construction of realistic P&R benchmark

Routability Prediction

(DATE 2023)

- Hierarchical DL model

(ICCAD 2023)

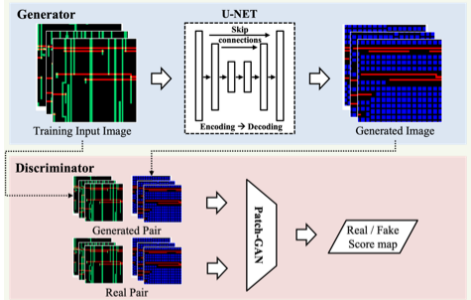
[SLIP 2023]

- XAI-based optimization

GAN-Dummy Fill

(GLS-VLSI 2022)

- Timing-aware dummy fill method using GAN
- Add loss terms for density and coupling cap



10 publications in 2023 *(TCAD 1, DATE 3, DAC 1, ISLPED 1, MLCAD 1, ICCAD 2, SLIP 1)*

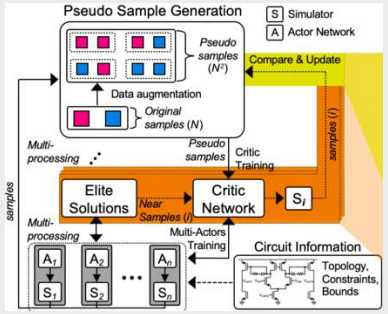
Recently-Published AI-EDA Works from POSTECH CSDL (2024)

Custom Design → **DTCO/DSO** → **Placement** → **Placement for Adv. Tech.** → **Sign-off**

MARL-based Analog Circuit Optimization

(TCAS I 2024)

- Break down complex circuits using multi-agent



TL-based Analog Circuit Optimization

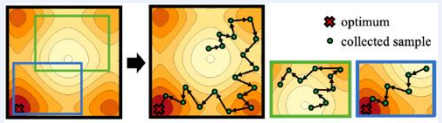
(DATE 2024)

- Transfer Learning (TL)

XAI for FPGA DSO

(DATE 2024)

- FPGA parameter DSO



RL-based BEOL Config. (DATE 2024)

- BEOL configuration pathfinding using RL

MARL to Improve PPA

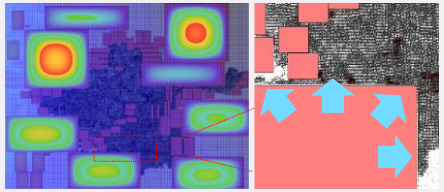
(ICCAD 2024)

- Multi-agent RL performs buffer insertion, gate sizing, Vth assignment

Mixed-size Placement

(DAC 2024)

- SkyPlace: Mixed-size Placement Framework
- GPU-accelerated



Clustering-driven Placement

(DAC 2024)

- PPA-aware clustering
- ML-accelerated virtualized P&R

Row-based Placement

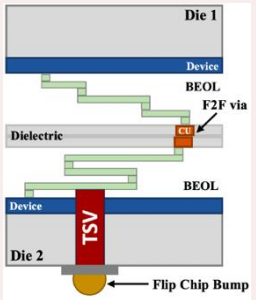
(DATE 2024)

- Mixed track-height std. cell placement with row-based design

3D-IC Placement

(MLCAD 2024)

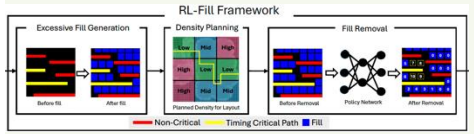
- Timing aware partitioning and placement

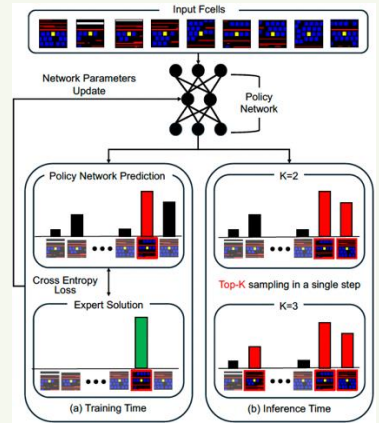


RL-based Metal Fill

(ICCAD 2024)

- Timing-aware metal fill with RL





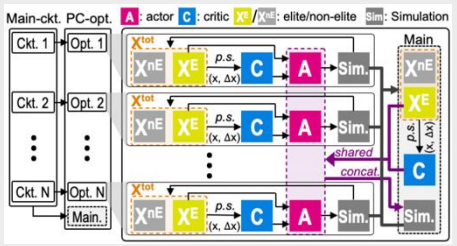
10 publications in 2024 *(TCAS I 1, DATE 4, DAC 2, MLCAD 1, ICCAD 2)*

Recently-Published AI-EDA Works from POSTECH CSDL (2025)

IC design → **DTCO/DSO** → **Placement** → **Security** → **Sign-off**

Complex Analog Circuits Optimization using Multi-Agents with Partition-and-Conquest Strategy

(ASP-DAC 2025)

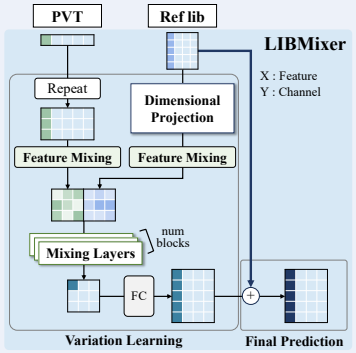


HDL Generation using LLMs with RL-based Fine-tuning

(DATE 2025)

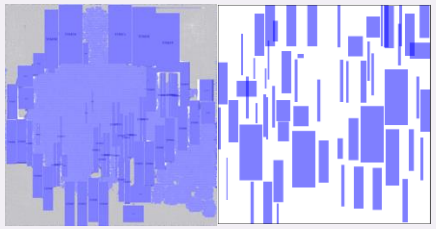
Std. Cell Library Characterization for DSO using ML

(ASP-DAC 2025)



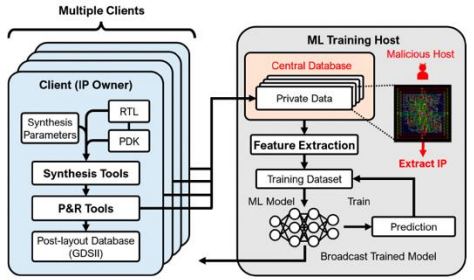
Macro Placement using Generative Diffusion Model

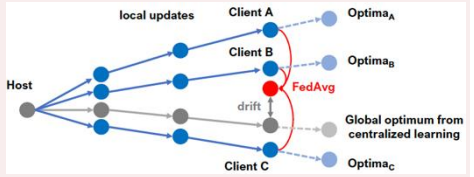
(DAC-LBR 2025)



Privacy-Preserving ML-EDA Prediction in Pre-route Stage using Federated Learning

(DAC 2025)



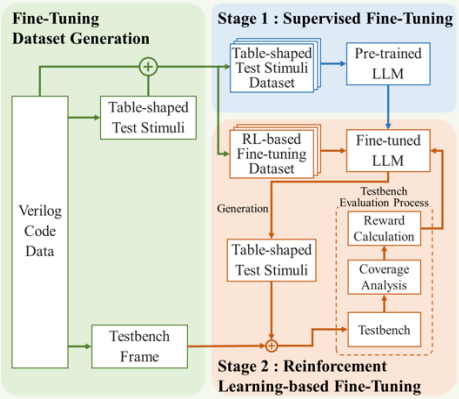


Parasitic RC Prediction using Heterogeneous GNN and Transformer

(ASP-DAC 2025)

Fine-tuning LLMs for Test Stimuli Generation

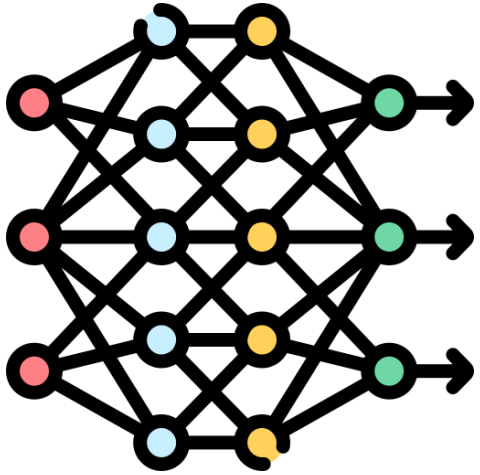
(DAC-LBR 2025)



7 publications in early 2025 *(DATE 1, ASP-DAC 3, DAC 3)*

2.
Deep Learning Hardware

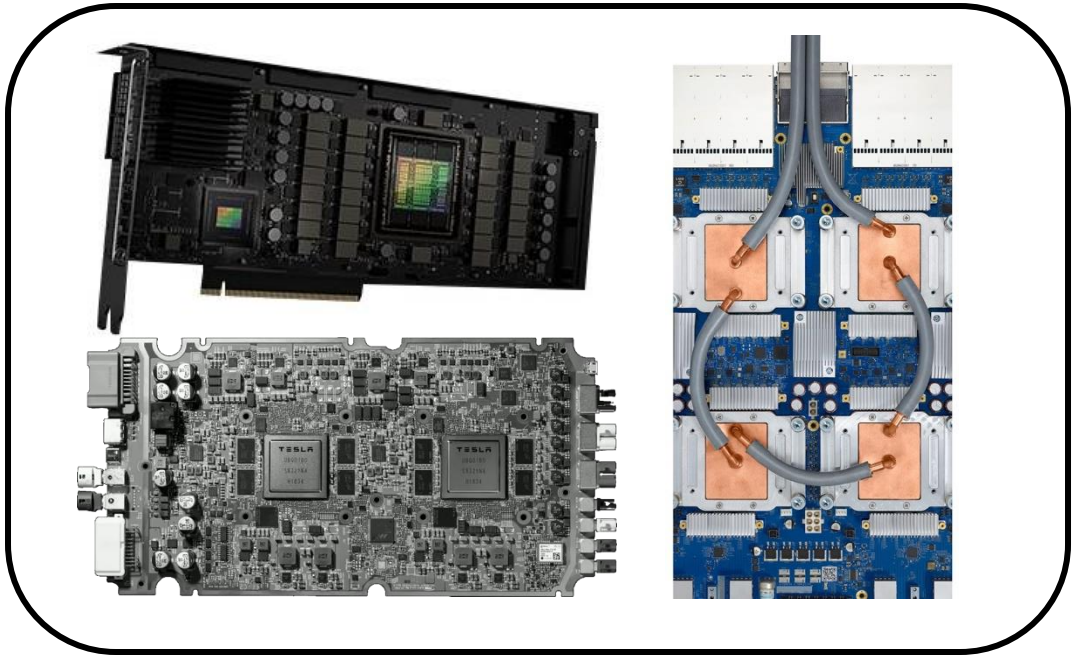
Deep Learning Hardware



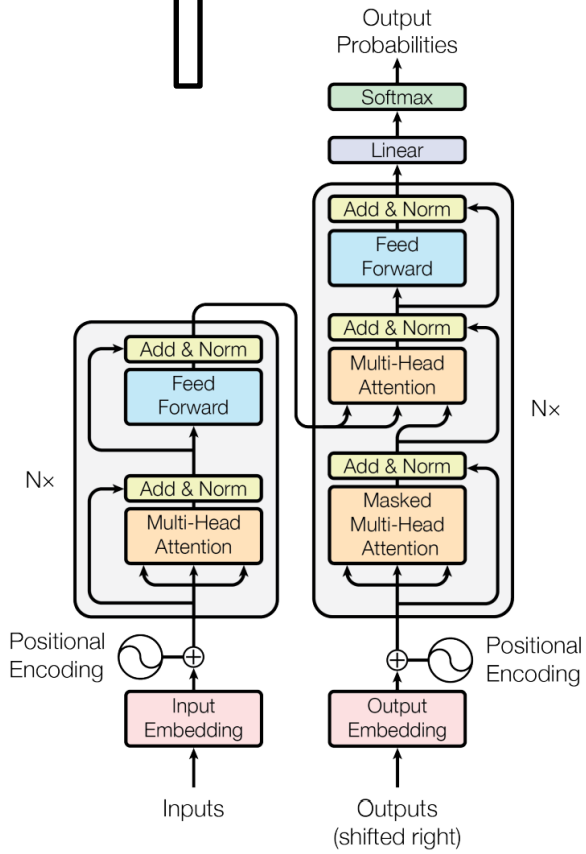
CNN

Inference

Training



Deep Learning HW

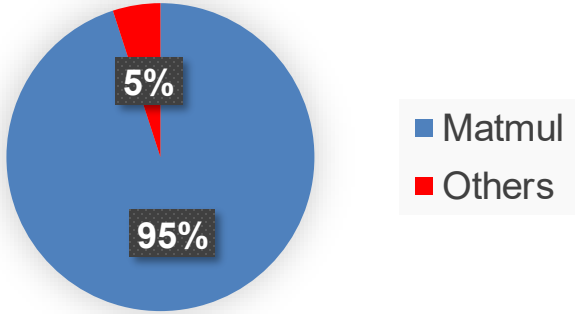


Transformer

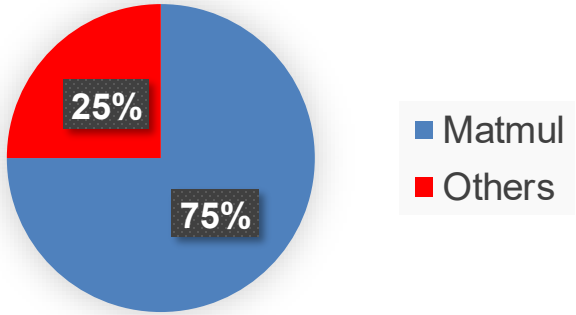
Why Deep Learning Hardware?

Ratio of Matmul

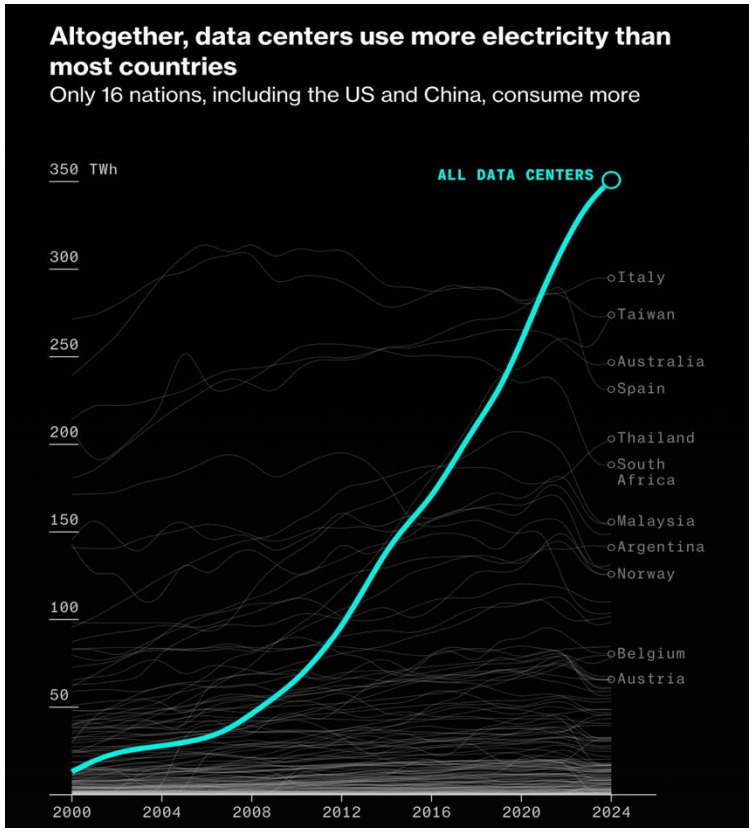
Parameters



Computations



Power Shortage Issue



Purpose-Specific HW

CPU
- Small models
- Small datasets
- Useful for design space exploration

GPU
- Medium-to-large models, datasets
- Image, video processing
- Application on CUDA or OpenCL

TPU
- Matrix computations
- Dense vector processing
- No custom TensorFlow operations

FPGA
- Large datasets, models
- Compute intensive applications
- High performance, high perf./cost ratio

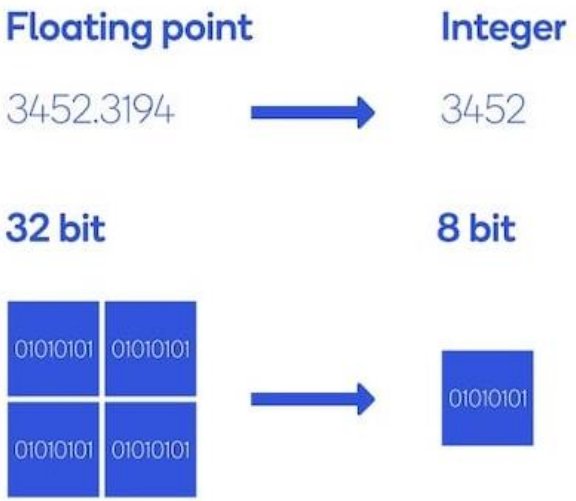
Matmul operation Acceleration & Energy efficiency are important → Specialized HW is necessary

T. Dettmers et al., "LLM.int8(): 8-bit Matrix Multiplication for Transformers at Scale" *NeurIPS*, 2022

Goal of Deep Learning Hardware

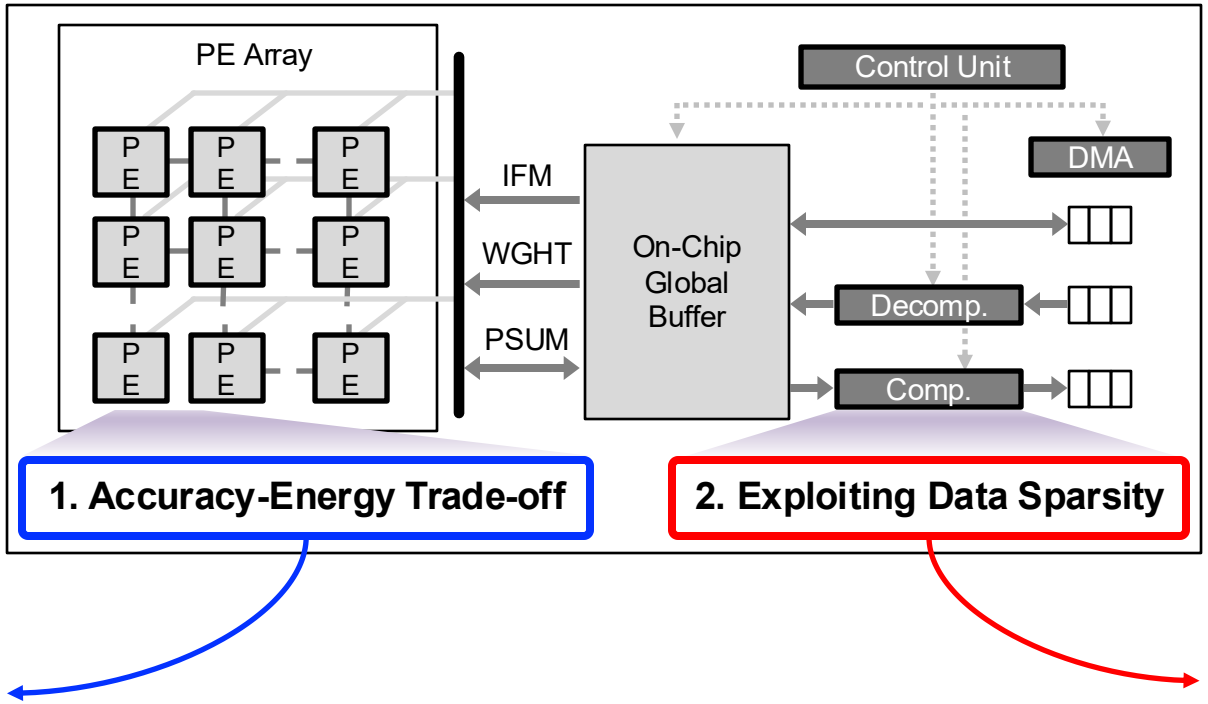
Accuracy ≈ Energy ↓

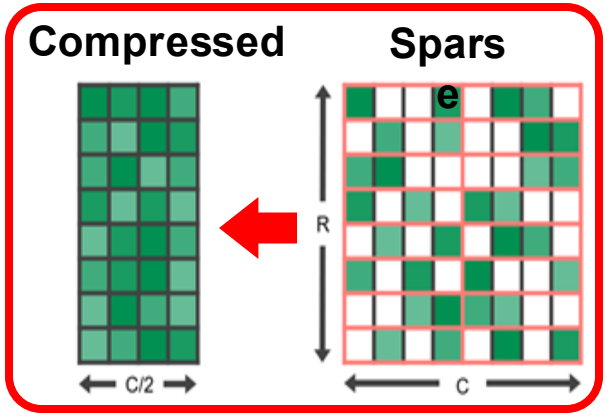
Quantization



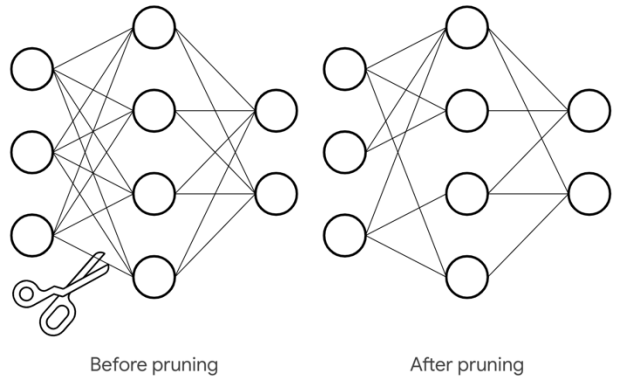
HW-SW Co-optimization

Should be supported by HW Accelerator!





Pruning



Recent AI HW Works from CSDL (http://csdl.postech.ac.kr)

RL-PTQ: RL-based Mixed Precision Quantization for Hybrid Vision Transformers

Eunji Kwon, Minxuan Zhou, Weihong Xu, Tajana Rosing and Seokhyeong Kang
2024 61th ACM/IEEE Design Automation Conference (DAC), **2024**

ViT-ToGo : Vision Transformer Accelerator with Grouped Token Pruning

Seungju Lee, Kyumin Cho, Eunji Kwon, Sejin Park, Seojeong Kim and Seokhyeong Kang
2024 IEEE/ACM Design, Automation and Test in Europe Conference & Exhibition (DATE), **2024**

Mobile Transformer Accelerator Exploiting Various Line Sparsity and Tile-based Dynamic Quantization

Eunji Kwon, Jongho Yoon, and Seokhyeong Kang
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), **2023**

FPGA-Based Accelerator for Rank-Enhanced and Highly-Pruned Block-Circulant Neural Networks

Haena Song, Jongho Yoon, Dohun Kim, Eunji Kwon, Tae-Hyun Oh, and Seokhyeong Kang
2023 IEEE/ACM Design, Automation and Test in Europe Conference & Exhibition (DATE), **2023**

Mobile Accelerator Exploiting Sparsity of Multi-Heads, Lines and Blocks in Transformer in Computer Vision

Eunji Kwon, Haena Song, Jihye Park, and Seokhyeong Kang
2023 IEEE/ACM Design, Automation and Test in Europe Conference & Exhibition (DATE), **2023**

Adaptive FSP: Adaptive Architecture Search with Filter Shape Pruning

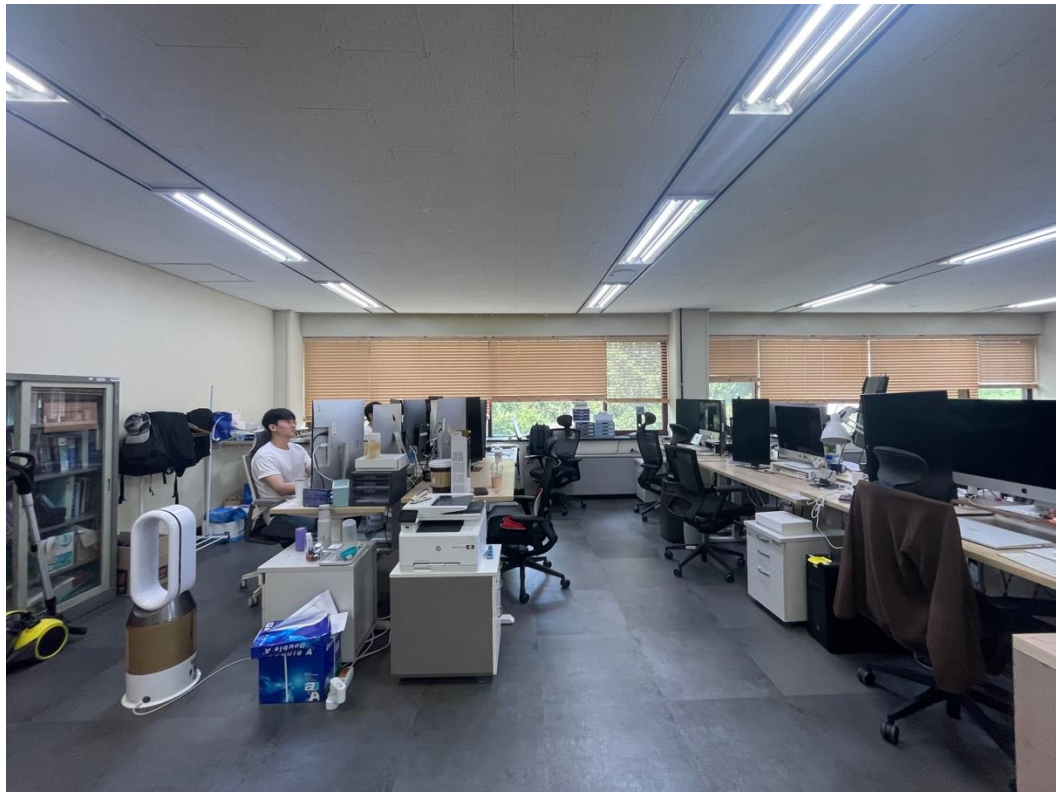
Aeri Kim, Seungju Lee, Eunji Kwon, and Seokhyeong Kang
The 16th Asian Conference on Computer Vision (ACCV), **2022**

Conclusion.
Why CSDL ?

Environment - Lab

LG 연구동 302호

공학 2동 405호



Environment - Equipment

- **Personal**
  - 5K iMac or High-end Window PC
  - DELL 4K27 Monitor 2x
  - Any Keyboard/Mouse you want

- **Server**
  - CPU server 4x
  - GPU server 7x
  - Storage server 3x

Funding Projects (국가과제)

- (IITP) DRAM PIM 설계 기반 기술개발 (~2026.2)
- (IITP) PIM 인공지능반도체 핵심 기술 개발 (~2027.2)
- (과기정통부) 칩렛 이종집적 초고성능 AI 반도체 개발 (~2027.12)
- (ERC) 확장형 양자컴퓨터 기술융합 플랫폼 센터 (~2027.2)
- (과기정통부) 미래기술연구실 (~2026.12)

과학기술정보통신부
Ministry of Science and ICT

NRF
한국연구재단
National Research Foundation of Korea

Funding Projects (기업과제)

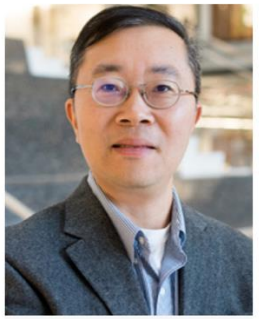
- **삼성전자**
  - Foundry 향 EDA tool: 회로 설계 최적화를 위한 Dummy Fill 연구
- **SK Hynix**
  - AI driven DRAM core Physical Design 자동화 툴 개발을 통한 센싱 마진 개선
- **LX 세미콘**
  - 데이터 증강 및 강화 학습을 활용한 LLM 기반 Verilog 코드 생성 개선
- **LIG 넥스원**
  - FPGA 기반 임베디드 자동 표적 인식 모델 개발 및 최적화
- **Google**
  - Open-source VLSI Placement Framework
- **AXION**
  - Standard cell layout auto-generation

International Conference

- ✓ ISPD 2019 (SF, US)
- ✓ ISMVL 2019 (Canada)
- ✓ DAC 2022 (San Francisco)
- ✓ ICCD 2022 (Lake Tahoe)
- ✓ ICCAD 2022 (San Diego)
- ✓ ASP-DAC 2023 (Tokyo, Japan)
- ✓ DATE 2023 (Antwerp, Belgium)
- ✓ DAC 2023 (San Francisco)
- ✓ ISLPED 2023 (Wien, Austria)
- ✓ MLCAD 2023 (Snowbird, Utah)
- ✓ ICCAD 2023 (San Francisco, US)
- ✓ DATE 2024 (Valencia, Spain)
- ✓ DAC 2024 (San Francisco, US)
- ✓ ICCAD 2024 (New Jersey, US)
- ✓ MLCAD 2024 (Utah, US)

International Research Collaborations

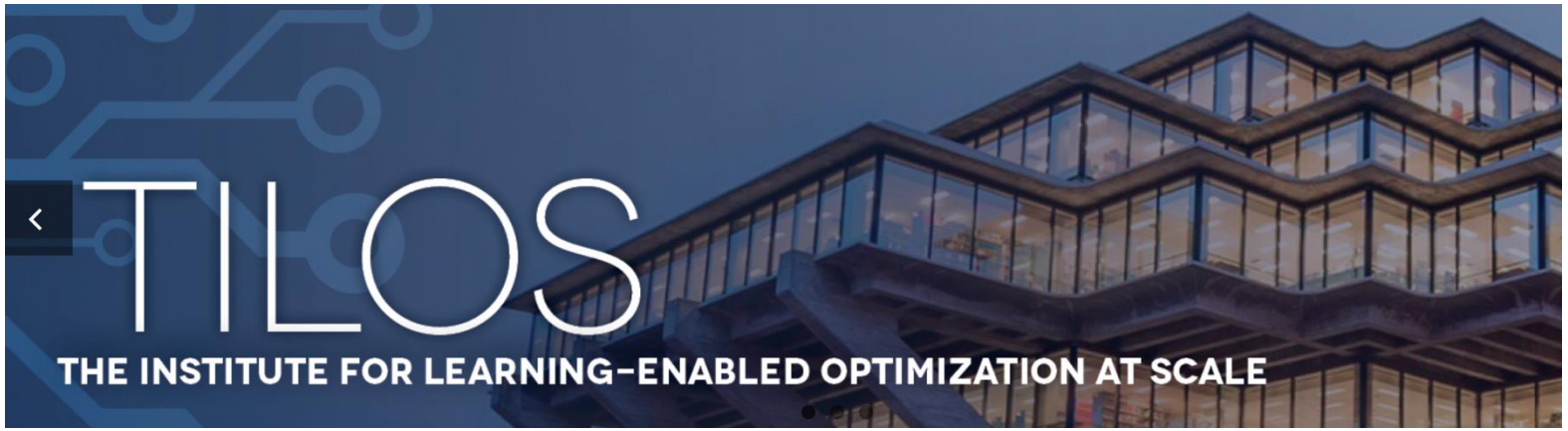

Andrew Kahng (co-lead)


David Pan (co-lead)


Sicun Gao


Farinaz Koushanfar


Tajana Rosing



- **Recent International Internship**
  - **2023. 8 ~ 2024. 2 UCSD, Prof. Tajana Rosing (권은지)**
  - **2023. 8 ~ 2024. 2 Technical Univ. of Munich, Prof. Robert Wille (박성혜)**
  - **2024. 5 ~ 2024. 11 UCSD, Prof. Andrew Kahng (박성현)**
  - **2024. 2 ~ 2025. 2 UCSD, Prof. Andrew Kahng (이자강)**

CSDL Workshop

CSDL EVENT

CSDL Alumni (PhD)

Sunghye Park
Assistant Professor at Ajou University from 2025

Eunji Kwon
Assistant Professor at Kookmin University from 2024

Sung-Yun Lee
Staff Researcher at AI Center in Samsung Electronics Co., Ltd. from 2025

Daeyeon Kim
Senior Researcher at Foundry Division of Samsung Electronics Co., Ltd. from 2023

Sunmean Kim
Assistant Professor at Kyungpook National University from 2023

Sangho Yoon
Senior Researcher at Semiconductor R&D center of Samsung Electronics Co., Ltd.

Hyun-Jeong Kwon
Senior Researcher at Electronics and Telecommunications Research Institute (ETRI)

CSDL Alumni (PhD)

Sodam Han
Senior Researcher at Foundry Division of Samsung Electronics Co., Ltd.

Ho Sub Lee
Assistant Professor at Kumoh National Institute of Technology from 2023

Yonghee Yun
Senior Researcher at Samsung Electronics Co., Ltd.

Gyu-Jin Bae
Senior Researcher at LG Display Co., Ltd.

Yesung Kang
Staff Engineer at System LSI Division of Samsung Electronics Co., Ltd.

Seungwon Kim
Lead Software Engineer at Cadence Design Systems Inc. in San Jose

CSDL Alumni (M.S)

Junseok Hur
Research Engineer at Memory Division of Samsung Electronics Co., Ltd. from 2025

Donggyu Kim
Research Engineer at SK hynix Inc. from 2025

Sejin Park
Senior Engineer at Synopsys Inc. in Pangyo, Korea from 2025

Minjae Kim
Researcher (Working as Military Service Exception) at Baum Design Systems Co., Ltd.

Seojeong Kim
Research Engineer at LG Electronics Inc.

Seungju Lee
Researcher at Korea Electronics Technology Institute (KETI) from 2024

Haena Song
Research Engineer at Samsung Research of Samsung Electronics Co., Ltd. from 2023

CSDL Alumni (M.S)

Jiyoung Min
Research Engineer at Memory Division of Samsung Electronics Co., Ltd. from 2023

Jihye Park
Research Engineer at Samsung Advanced Institute of Technology (SAIT) from of Samsung Electronics Co., Ltd. 2023

Minjeong Choi
Research Engineer at Samsung Advanced Institute of Technology (SAIT) from of Samsung Electronics Co., Ltd. from 2023

Seunggyu Lee
INVESTORS(SEED/SERIES A) TEAM at BluepointPartners

Chanhee Lee
Research Engineer at LG Electronics Inc.

Myong Kong
Senior Researcher at SK hynix Inc.

CSDL Alumni (M.S)

Seunghan Baek
Research Engineer at Foundry Division of Samsung Electronics Co., Ltd. from 2022

Eunsik Kim
Research Engineer at Atlas Lab Inc.

Sunghoon Kim
Research Engineer at Foundry Division of Samsung Electronics Co., Ltd. from 2020

Yoonho Park
Technical Research Personnel at Anapass Inc.

Taeho Lim
Research Engineer at SK hynix Inc. from 2018

Mingyu Woo
Senior Engineer at Qualcomm Technologies Inc. in San Diego

CSDL Awards

Jaemin Seo, Jinoh Cho : **Excellence Prize & Encouragement Prize, Research Performance Contest of POSTECH-EE 2025**

Jaemin Seo, Sejin Park and Joonyoung Seo : **Synopsys Award, ISOCC 2024**

Kyungjun Min, Seonghyeon Park and Hyeonwoo Park : **Best Poster Award, ISOCC 2024**

Seonghyeon Park : **Excellence Prize, Research Performance Contest of POSTECH-EE 2024**

Haena Song, Dohun Kim, Jongho Yoon, and Eunji Kwon : **Bronze Prize, the 29th Samsung Humantech Paper Award**

CSDL Awards

Sunghye Park : **BEST prize, the Research Performance Contest of POSTECH EE 2023**

Dohun Kim, Sunghye Park, and Jaekyung Im : **QML Overall Challenge 1st Place Award, qBraid HAQS 2022**
Dohun Kim : **Excellence Award, IonQ & QCenter Quantum Challenge 2022**

Jaemin Seo : **Honorable Mention, ISPD 2022**

Chanhee Lee : **Best Poster Award, ISOCC 2021**

Jongho Yoon : **Best Poster Award, 28th KCS**

CSDL Openings

Openings for graduate courses

(2024. Spring)

- Regular program: 2 openings
- Sports AIX program: 1 openings
- PSEP program: 1 opening

POSTECH 입학처 일반대학원

37673 경상북도 포항시 남구 청암로 77 포항공과대학교 입학팀 / tel: 054-279-3783

admission.postech.ac.kr

https://admission.postech.ac.kr/mainUsko.do

Thank You !

CAD & SoC Design Lab